MAXBLUE USER GUIDE

MaxBlue User Guide

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Introduction

MaxBlue features the Maxim MAX32666 high-efficiency ARM® microcontroller and audio DSP for Bluetooth 5 Low Energy Radio connectivity. The GRBTM series provides an I/O breakout that allows for low cost carrier PCBs versus using the MAX32666 directly. Featuring an FCC Modular Certification, the GRBTM series enables a short prototyping cycle direct to a product that can meet FCC requirements for sale without additional certification testing.

This modular series breaks out all interfaces and features of the MAX32666 including; USB High Speed, secure digital, SPI, UART, and I2C. The module also provides an audio subsystem supporting PDM, I2S, and TDM interfaces. See the Maxim MAX32666 documentation for a complete list of peripherals.

The module comes in one of two variations depending on the antenna. The first variant is the GRBTM-ANT, which comes equipped with a low-profile surface mount chip antenna with peak performance in the 2.4GHZ BT range. Modules with on-board antennas require the physical placements and mechanical details of the integrated board to closely match the evaluation board in order to achieve the stated performance.

The second variant in the series, the GRBTM-NANT, provides a breakout pad for connecting a customer-supplied antenna to the module's RF transmission line. This variant allows for the use of the best performing and optimized antenna for your specific product requirements.

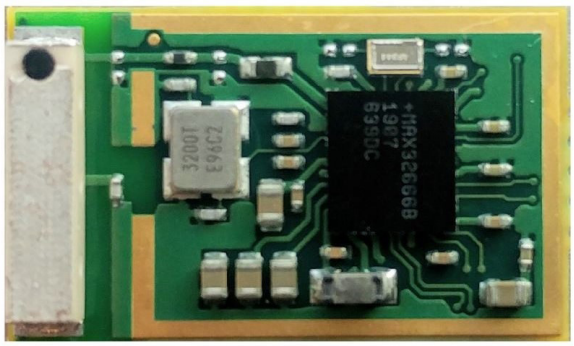

Figure 1: The GRBTM-ANT-01 module without the shield.

Variants

GotRad PN	Description
GRBTM-ANT	The GotRad Module with embedded chip antenna.
GRBTM-NANT	The GotRad Module with pad connected to the transmission line for customer antenna integration.
GRBTM-EVA	The GotRad Module, GRBTM-ANT, embedded on a development board.
GRBTM-EVNA	The GotRad Module, GRBTM-NANT, embedded on a development board populated to support an SMA terminal antenna.

Dimensions

Length	GRBTM-ANT-01 • Length: 16.5mm GRBTM-NANT-01 • Length: 13.3mm
Width	10.1mm
Weight	1g

References

1. **MAX32665-MAX32668 Data Sheet**

Features

Bluetooth 5 Low Energy Radio	• Up to 2Mbps Data Throughput • Long Range: 125kbps - 500kbps • Rx Sensitivity: -95dbm • Tx Power: +9.5dbm
Microcontroller Features	• Arm Cortex-M4 with FPU Up to 96MHz • Low-Power 7.3728MHz System Clock Option • 1MB Flash, Organized into Dual Banks 2 x 512KB • 560KB (448KB ECC) SRAM; 3 x 16KB Cache • Optional Error Correction Code (ECC-SEC-DED) for Cache, SRAM, and Internal Flash

Interfaces	The module contains multiple peripherals for system control.
	• Three QSPI Master/Slave with three chips selects each
	  ○ QSPI SPIXF with Real-Time Flash Decryption
	  ○ QSPI SPIXR RAM Interface Provides SRAM Expansion
	• Three 4-wire UARTs
	• Three I² C Master/Slave
	• USB 2.0 HS Engine with internal transceiver
	• PDM interface supports two digital microphones
	• I² S with TDM
	• 1-Wire Master
	• 8-input, 10-bit Delta-Sigma ADC at 7.8ksps
	• Secure Digital Interface Supports SD3.0/SDIO3.0/eMMC4.51
	• See the Maxim MAX32666 documentation for a complete list of peripherals.

Secure Valuable IP/Data with Hardware Security	• Trust Protection Unit (TPU) with MAA Supports Fast ECDSA and Modular Arithmetic • AES-128, -192, -256, DES, 3DES, Hardware Accelerator • TRNG Seed Generator, SHA-2 Accelerator • Secure Bootloader
Module Clocks	The GRBTM series comes equipped with two additional oscillators. • 32 MHz • 32.768 kHz
Antenna	• Onboard Low Profile Ceramic Surface Mount Antenna ○ 2.4 GHz Embedded Loop Chip Antenna ○ Antenna Dimensions: 8mm x 2mm x 2mm • Available RF pad for Customer Supplied Antenna (pin 61)
Supported Band	• 2.4 GHz ISM band with support for worldwide power and band edge limits
Environmental Conditions	• Operating Temperature Range ○ -40°C to +85°C
Power	• Supply Voltage ○ 2.0V-3.6V, **+3.3VDC Recommended**
Approvals	• FCC - USA • IC - Industry Canada

Functional Architecture

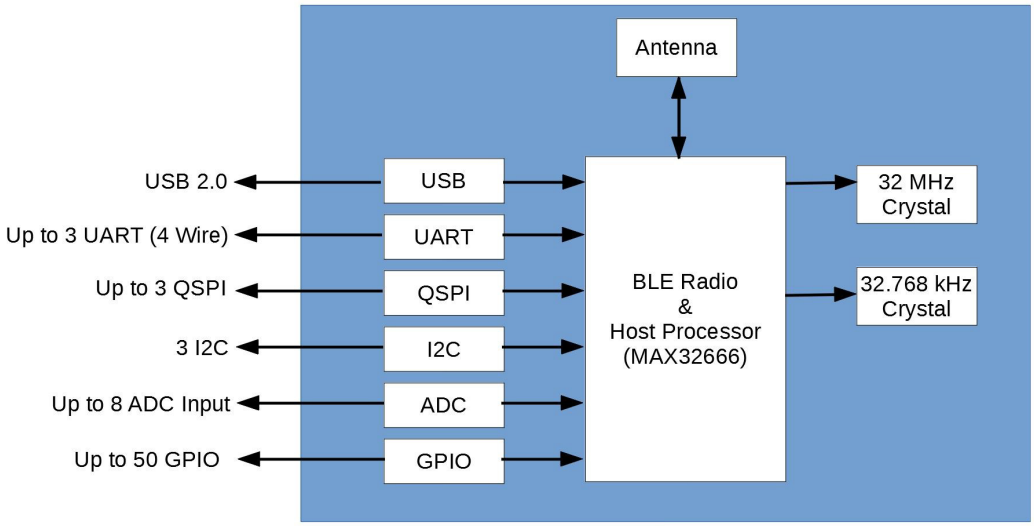

Figure 2: Block Diagram

Pinout Functions

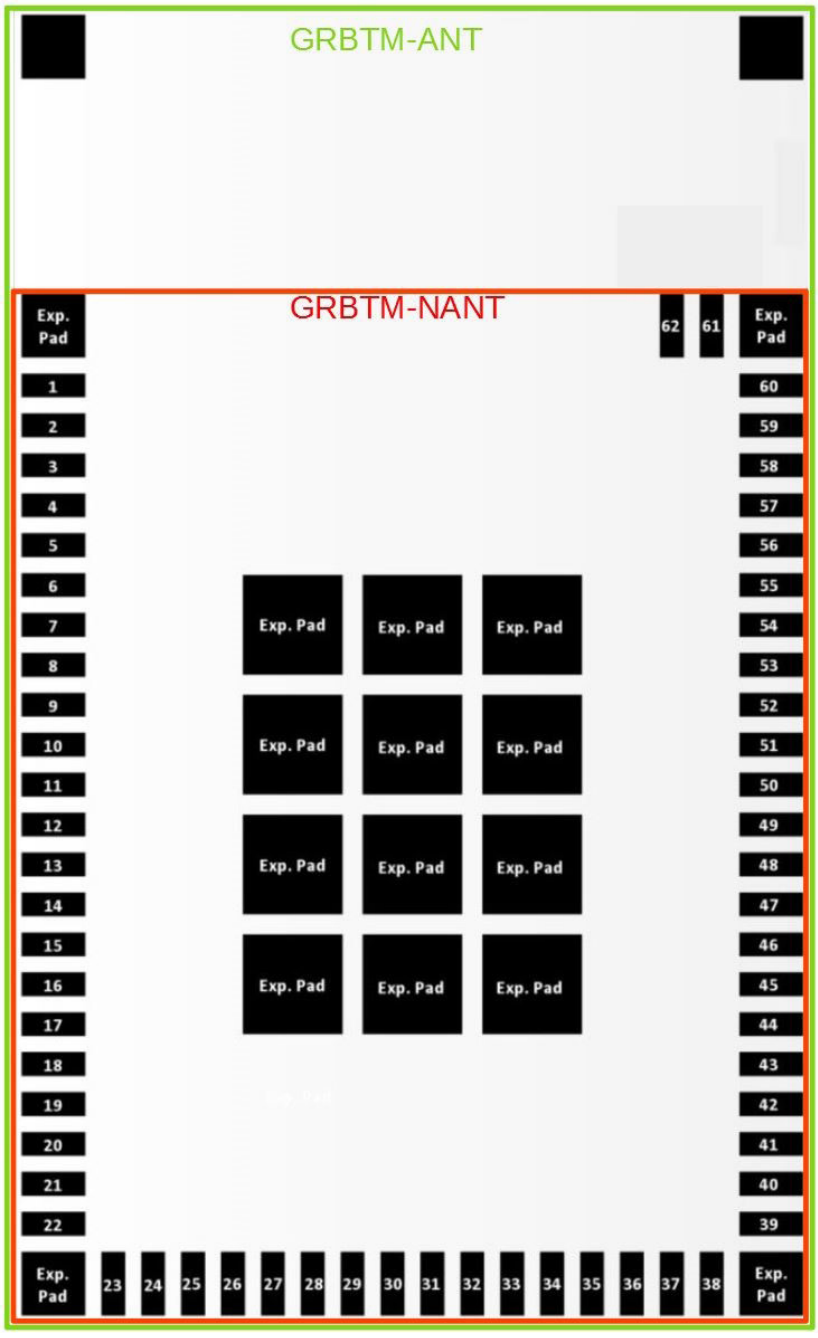

Figure 3: Module Pinouts.

Pin	Name	Function
1	P0.11	SPIXR_SCK/ QSPI0_SCK/ UART0_RTS/ TMR5
2	P0.15	I2C1_SDA/ QSPI0_SS2/ BLE_ANT_CTRL/ TMR3
3	P0.8	SPIXR_SS0/ QSPI0_SS0/ UART0_CTS/ TMR2
4	P0.21	AIN5, AIN2N/ QSPI1_SDIO3/ UART1_TX/ TMR3
5	P0.24	PCM_LRCLK/ QSPI2_SS0/ OWM_IO/ TMR0
6	P0.25	PCM_DOUT/ QSPI2_MOSI/ SDIO0/ OWM_PE/ TMR1
7	P0.14	I2C1_SCL/ QSPI0_SS1/ BLE_ANT_CTRL/ TMR2
8	P0.27	PCM_BCLK/ QSPI2_SCK/ TMR3/ SQWOUT
9	P0.29	PDM_DATA3/ QSPI2_SDIO3/ UART2_TX/ TMR5

Pin	Name	Function
10	P0.13	SPIXR_SDIO3/QSPI0_ SDIO3/OWM_PE/TMR1
11	P0.9	SPIXR_MOSI/SDIO0/QSPI0_ MOSI/SDIO0/UART0_TX/ TMR3
12	P0.23	AIN7/AIN3N/QSPI1_SS2/ UART1_RTS/TMR5
13	P0.12	SPIXR_SDIO2/QSPI0_ SDIO2/OWM_IO/TMR0
14	P0.19	AIN3/AIN1N/QSPI1_SCK/ TMR1/SQWOUT
15	P0.20	AIN4/AIN2P/QSPI1_SDIO2/ UART1_RX/TMR2
16	P0.16	AIN0/AIN0P/QSPI1_SS0/ OWM_IO/TMR4
17	VDD_USB	VDD_USB
18	USB_N	USB_N
19	USB_P	USB_P
20	GND	GND
21	SWDIO	SWDIO
22	SWCLK	SWCLK
23	VCC	VCC
24	VCC	VCC
25	GND	GND
26	RESET#	RESET#
27	P0.2	SPIXF_MISO/SDIO1/UART2_ RX/TMR2

Pin	Name	Function
28	P0.4	SPIXF_SDIO2/OWM_IO/TMR4
29	P0.5	SPIXF_SDIO3/OWM_PE/TMR5
30	P0.6	I2C0_SCL/SWDIO2/TMR0
31	P0.7	I2C0_SDA/SWCLK2/TMR1
32	P0.1	SPIXF_MOSI/SDIO0/UART2_TX/ TMR1
33	P0.0	SPIXF_SS0/UART2_CTS/ TMR0
34	P0.22	AIN6/AIN3P/QSPI1_SS1/ UART1_CTS/TMR4
35	P0.18	AIN2/AIN1P/QSPI1_MISO/SDIO1/ TMR0/PDOWN
36	P0.17	AIN1/AIN0N/QSPI1_MOSI/SDIO0/ OWM_PE/TMR5
37	P0.3	SPIXF_SCK/UART2_RTS/TMR3
38	P0.31	PDM_MCLK/QSPI2_SS2/UART2_ RTS/TMR1
39	P0.26	PCM_DIN/QSPI2_MISO/SDIO1/ TMR2/PDOWN
40	P0.28	PDM_DATA2/QSPI2_SDIO2/ UART2_RX/TMR4
41	P0.30	PDM_RX_CLK/QSPI2_SS1/ UART2_CTS/TMR0
42	P0.10	SPIXR_MISO/SDIO1/QSPI0_MISO/ SDIO1/UART0_RX/TMR4
43	P1.2	SDHC_DAT0/SDMA_TDI/PT2
44	P1.3	SDHC_CLK/SDMA_TCK/PT3
45	P1.1	SDHC_CMD/SDMA_TDO/PT1

Pin	Name	Function
46	NC	NC
47	P1.7	SDHC_CDN/UART0_RTS/PT7
48	P1.4	SDHC_DAT1/UART0_RX/PT4
49	P1.5	SDHC_DAT2/UART0_TX/PT5
50	P1.0	SDHC_DAT3/SDMA_TMS/PT0
51	P1.8	QSPI0_SS0/PT8
52	P1.6	SDHC_WP/UART0_CTS/PT6
53	P1.10	QSPI0_MISO/PT10
54	P1.14	I2C2_SCL/UART1_CTS/PT14/ JTAG TDI
55	P1.9	QSPI0_MOSI/PT9
56	P1.15	I2C2_SDA/UART1_RTS/PT15/ JTAG TDO
57	P1.11	QSPI0_SCK/PT11
58	P1.12	QSPI0_SDIO2/UART1_RX/ PT12
59	P1.13	QSPI0_SDIO3/UART1_TX/ PT13
60	GND	GND
61	RF_OUT	RF_OUT
62	GND	GND
63-78	EXP_PAD	EXP_PAD
79-80	ANT_PAD	ANT_PAD

Interfaces

Serial Communications Overview

- Baud rate generation with ±2% optionally utilizing the 7.3727MHz relaxation oscillator
- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Maximum baud rate 4000 kB
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

- The following features are supported:
  - USB Device Mode
  - USB 2.0 Full-Speed (FS) 12Mbps transfers
  - USB 2.0 Hi-Speed (HS) 480Mbps transfers
  - Bulk transfers
  - Isochronous transfers
  - 11 endpoints plus Endpoint 0, each with dedicated FIFOs
  - Packet splitting and combining
  - High bandwidth IN and OUT Isochronous endpoints

- Each endpoint has an associated FIFO with the following sizes:
  - Endpoint 0 FIFO: 64 bytes deep
  - Endpoints 1 through 7 FIFOs: 512 bytes deep
  - Endpoints 8 and 9 FIFOs: 2048 bytes deep
  - Endpoints 10 and 11 FIFOs: 4096 bytes deep

- Supported interrupts include:
  - Interrupts for each IN endpoint from Endpoint 0 to Endpoint 11
  - Interrupts for each OUT endpoint from Endpoint 1 to Endpoint 11
  - Start of Frame (SOF)
  - RESET bus state
  - RESUME bus state
  - SUSPEND Mode bus state
  - STALL sent
  - Control byte received
  - Control transfer ended early
  - Packet transmitted
  - Packet received

  - Data underrun
  - Data overrun
  - Invalid token received
  - Empty data packet sent

- Master or slave mode operation
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed buses
- Multiple transfer rates
  - Standard mode: 100 kbps
  - Fast mode: 400 kbps
  - Fast mode plus: 1000 kbps
  - High-speed mode: 3400 kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

- Up to 48MHz operation in mode 0 and 3
- Single Slave Select
- Four wire mode for single-bit slave device communication
- Dual and Quad I/O supported
- Programmable Serial Clock (SCK) frequency and duty cycle
- Slave select assertion and de-assertion timing with respect to the leading and trailing SCK edge
- Configurable command, address, dummy, and data fields to support a variety of SPI flashes

The SPIXF allows the CPU to transparently execute instructions stored in an external SPI flash. Instructions fetched using the SPIXF are cached just like instructions fetched from internal program memory. You can also use the SPIXF to access large amounts of external static data that would otherwise reside in internal data memory. This device provides support for a wide variety of external SPI flash memory devices.

Prior to using the SPI flash device, you must configure the SPIXF interface.

- Four SPI modes (mode 0, 1, 2, and 3)
- Master mode only support
- Dual SPI Mode with two bidirectional serial data I/O (SDIO) lines
- High Performance Quad SPI Mode with four bidirectional SDIO lines
- Programmable Serial Clock (SCK) frequency and duty cycle with 48MHz maximum
- 32-byte Transmit FIFO, 32-byte Receive FIFO with DMA support backed by a 16KB Data Cache

The SPIXR Master Controller allows the CPU to transparently execute instructions stored in an external SPI SRAM device. Instructions fetched using the SPIXR Master Controller are cached just like instructions from internal program memory. You can also use the SPIXR Master Controller to access large amounts of external data that would otherwise reside in internal data memory.

Prior to using the SPI SRAM device, you must configure the SPIXR interface.

The command used to transfer SPI SRAM data is configured using firmware. Then, the access to SPI SRAM space (either code execution or data) may be performed by firmware. The AHB transaction initiated by the firmware provides address and other transaction critical parameters to control the data transfer from the external SPI SRAM.

- Flexible, 1-Wire timing generation (required 1 MHz timing base) using the OWM module clock frequency, which is in turn derived from the current system clock source. You can also prescale the OWM module clock to allow proper 1-Wire timing generation using a range of base frequencies.
- Automatic generation of proper 1-Wire time slots for both standard and overdrive timing modes.
- Flexible configuration for 1-Wire line pullup modes: options for internal pullup, external fixed pullup, and optional external strong pullup are available.
- Long-line compensation and bit banging (direct firmware drive) modes.
- 1-Wire reset generation and presence-pulse detection.
- Generation of 1-Wire read and write time slots for single-bit and eight-bit byte transmissions.
- Search ROM Accelerator (SRA) mode, which simplifies the generation of multiple-bit time slots and discrepancy resolution required when completing the Search ROM function to determine the IDs of multiple, unknown 1-Wire slaves on the bus.
- Transmit data completion, received data available, presence pulse detection, and 1-Wire line-error condition interrupts.

  Pin functions: OWM_PE is the 1-Wire Master Pullup Enable

- Single 4-wire I2S PCM interface allowing transmit and receive of audio data and is intended to connect to speaker driver devices
- Four transmit channels and eight receive channels are supported to allow 4-channel DSM
- Supports two PDM receive channels at the same time as PCM support
- Sample rates from 8 kHz to 192 kHz
- Up to two PDM transmit channels at 3.072 MHz
- Up to two PDM receive channels at 3.072 MHz
- Interpolation and decimation filtering to save MIPS in the DSP

Bluetooth 5 Low Energy (BT5 LE) Radio

Devices using bluetooth operate in the unlicensed 2.4 GHz ISM (Industrial, Scientific, Medical) band at 2400 MHz–2483.5 MHz. A frequency-hopping transceiver is used to combat interference and fading. It uses 40 RF channels that have center frequencies 2402 + k x 2 MHz, where k = 0, ..., 39.

The Maxim Bluetooth Module utilizes the latest version of the Bluetooth wireless communication standard, BT5 LE. The features of BT5 LE include:

- 1Mbps, 2Mbps, and Long-Range coded (125 kbps and 500 kbps) data rates
- Increased broadcast capability
- Advertising packet up to 255 bytes
- On-chip matching network to the antenna
- Provides hardware on-the-fly encryption and decryption for lower power consumption
- Supports mesh networking

- Supports high-quality audio streaming (isochronous)
- Low-power proprietary mode that supports 20 kbps, 40 kbps, 500 kbps-MSK/GFSK, 1Mpbs-GFSK

The provided BLE radio is optimized for low-power operation with the following power specifications:

- Higher transmit power up to +9.5dbm
- Low transmit current of 4.3mA at 0dBm at 3.3V
- Low receive current of 3.2mA at 3.3V

The receiver sensitivity with non-ideal transmitter for the BLE radio is:

- 1Mbps: -94dBm
- 2Mbps: -91dBm

Embedded Antenna Characteristics

The data below was collected with the module embedded on the development board. To achieve the performance shown, the module must be embedded to a board with similar dimensions, position, and PCB cutout beneath the antenna. The position on the development board and dimensions are shown in the figure below.

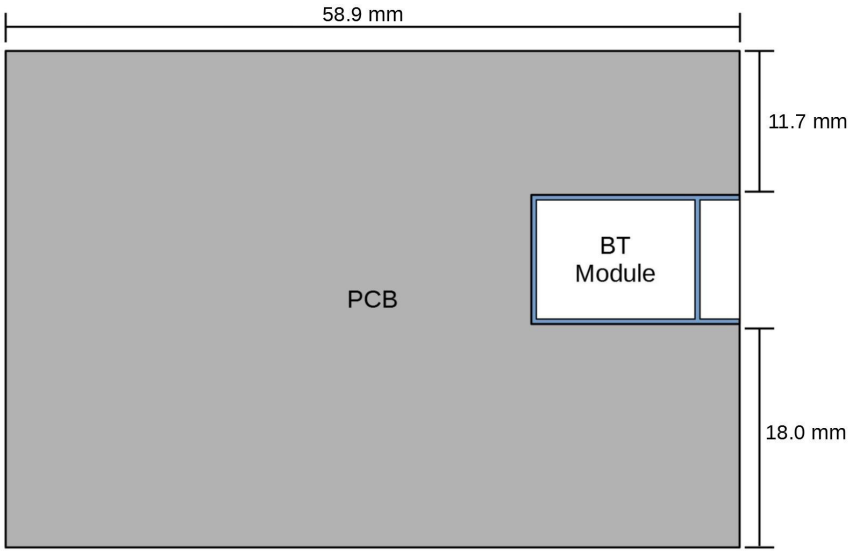

Figure 4: The position and orientation of the module relative to the development board on which the antenna performance was tested. This is the recommended mounting for the embedded chip antenna module.

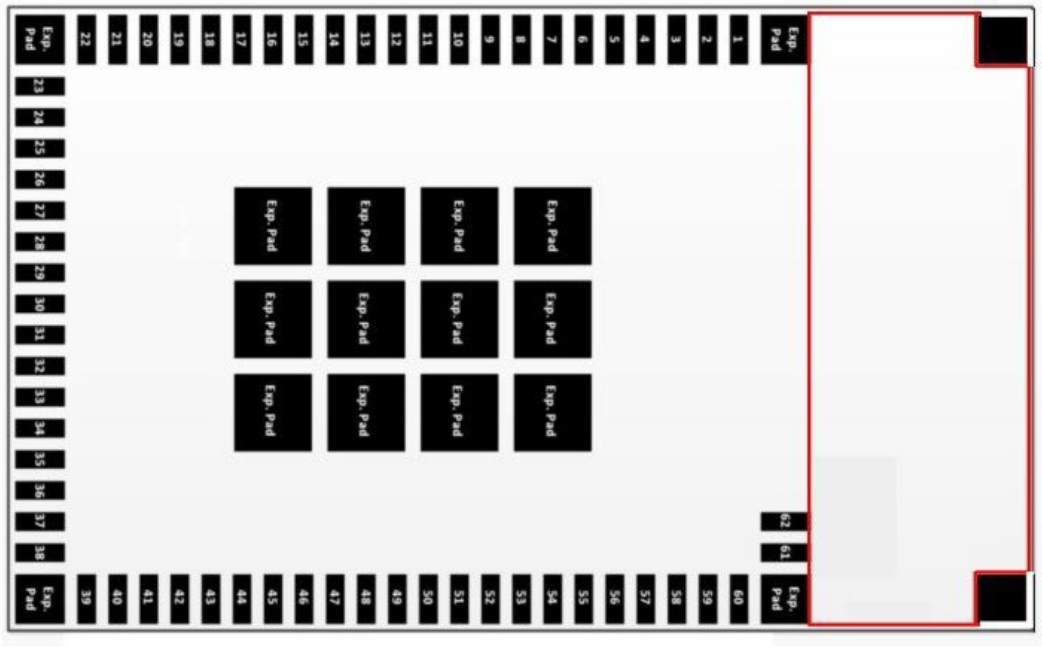

Figure 5: The figure above shows the recommended PCB copper cutout area in red. This cutout has been done in the module and should be done on the integration board. The square coroner pads connect directly to ground.

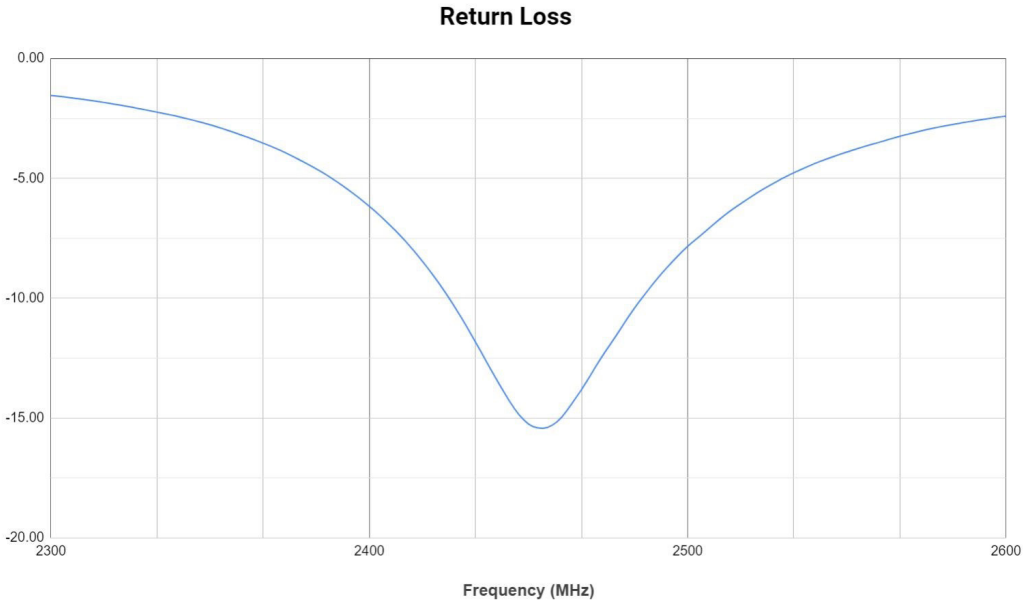

Figure 6: Antenna Return Loss

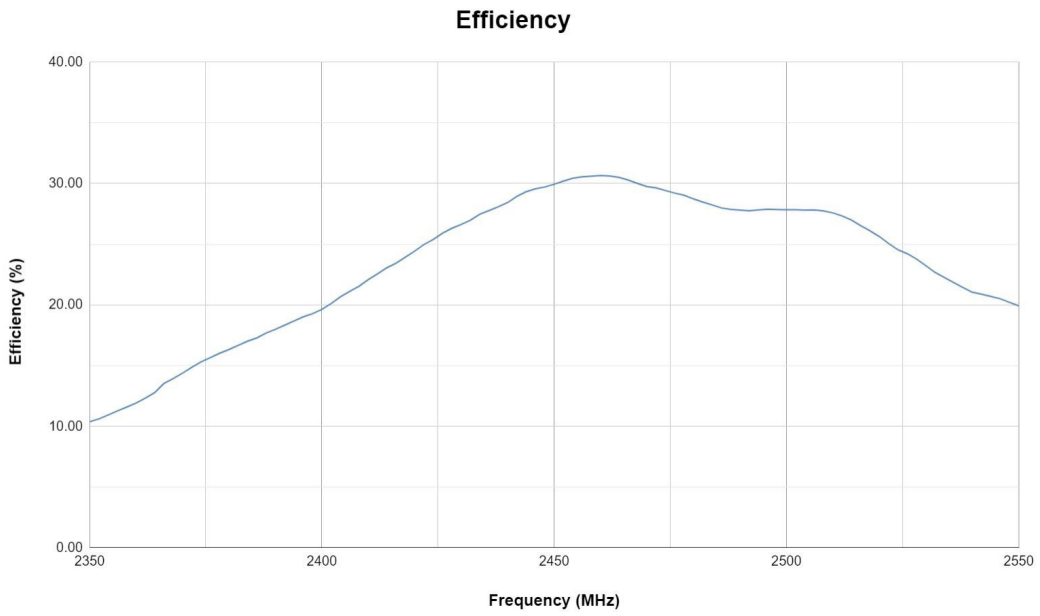

Figure 7: Antenna Radiation Efficiency

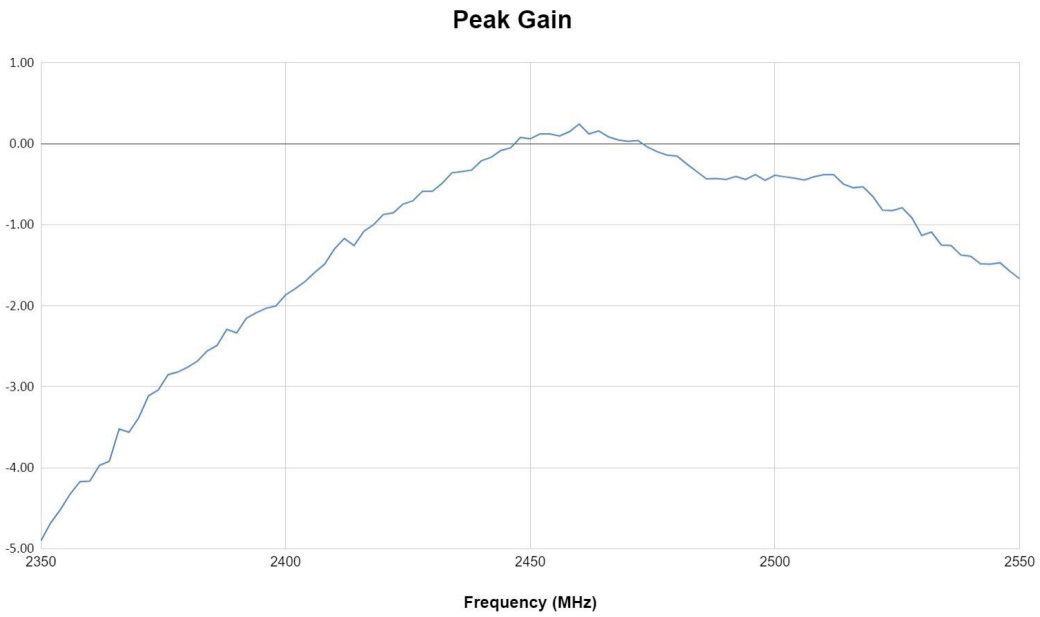

Figure 8: Antenna Peak Gain as a Function of Frequency

Radiation Plots

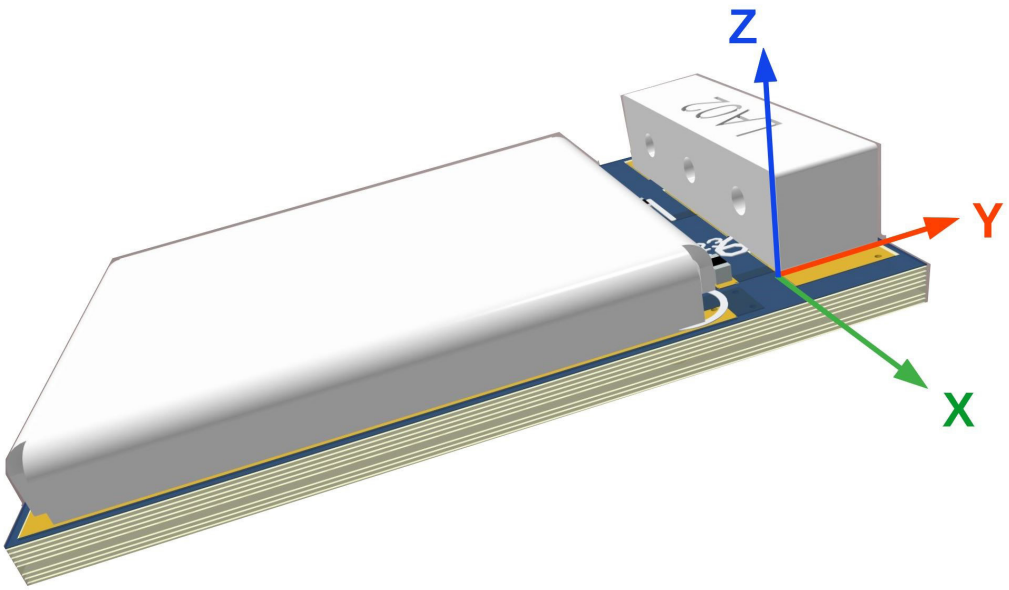

Figure 9: Module orientation for radiation plots:

2400 MHz

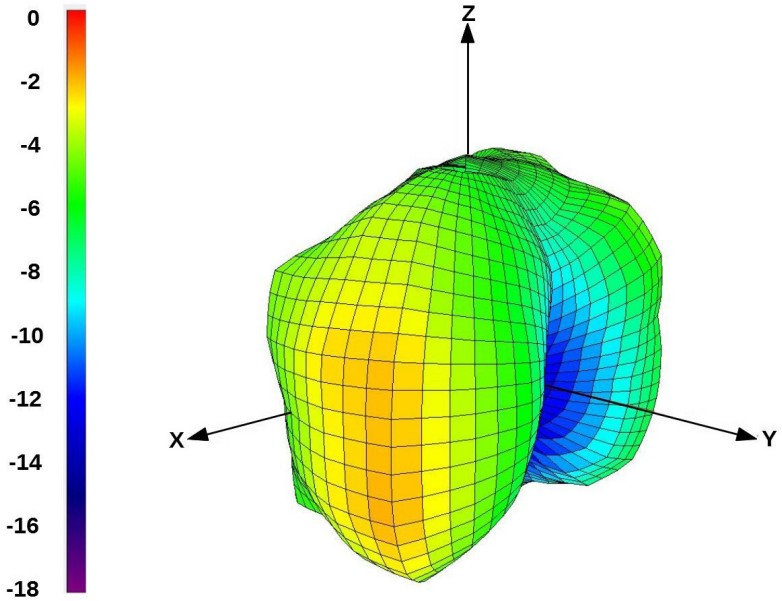

Figure 10: Low Channel Radiation Plot

2440 MHz

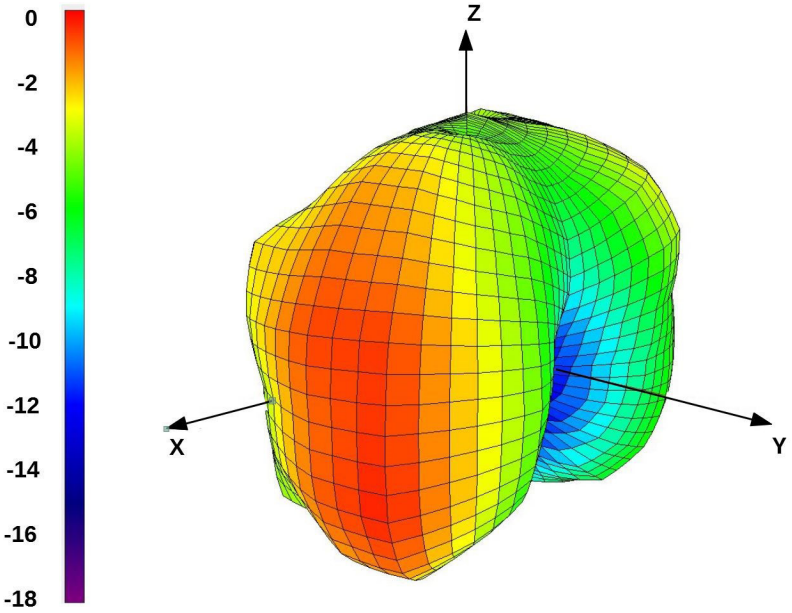

Figure 11: Mid-Channel Radiation Plot

2480 MHz

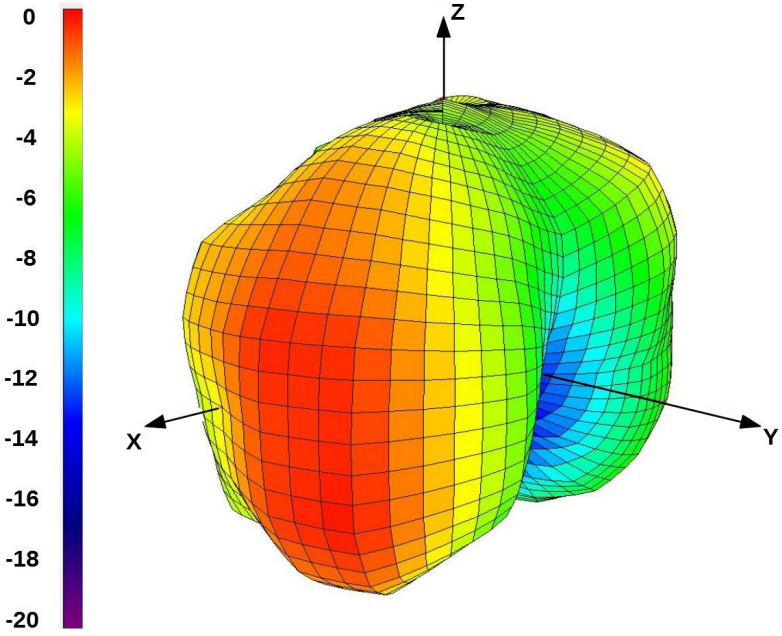

Figure 12: High Channel Radiation Plot

Mechanical Dimensions

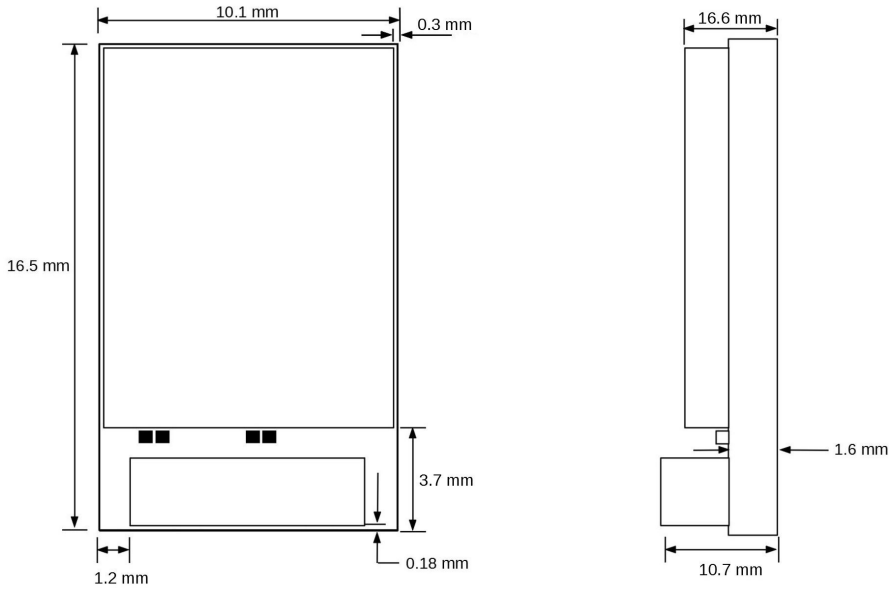

Figure 13: The mechanical dimensions of the GRBTM-ANT module including the shield..

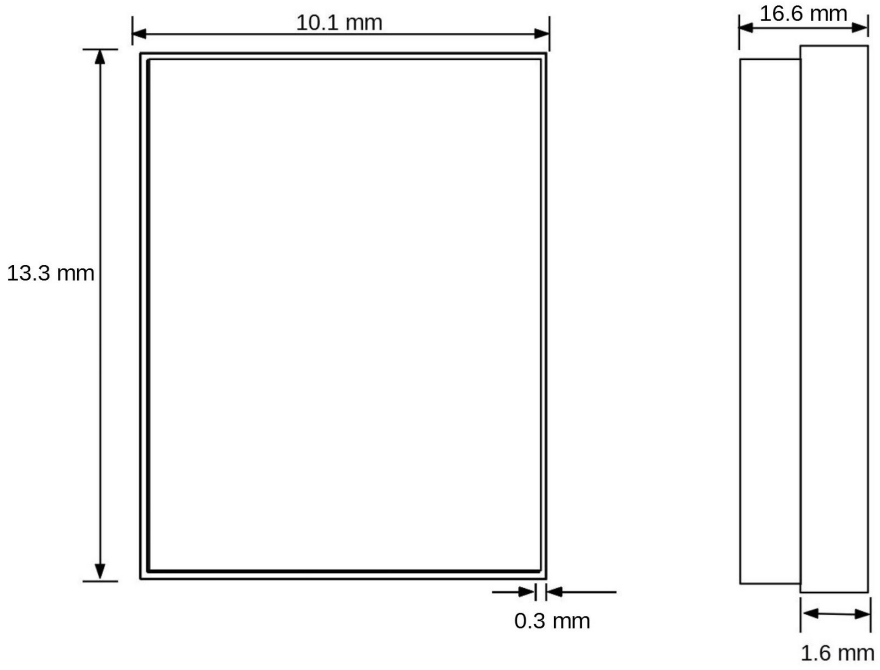

Figure 14: The mechanical dimensions of the GRBTM-NANT module including the shield. This figure has the same orientation as the previous mechanical diagram.

Footprint

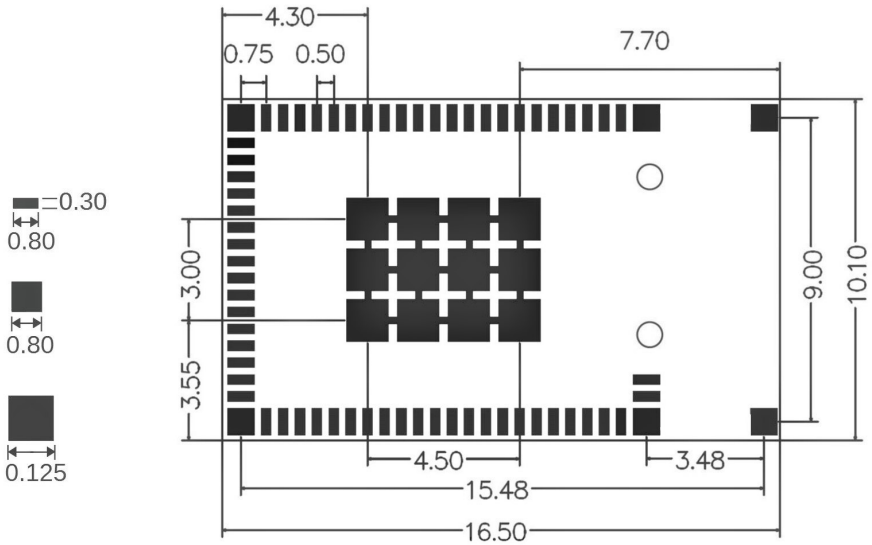

Figure 15: The footprint for the GRBTM-ANT is shown above.
All measurements are in millimeters For the GRBTM-NANT variant, the footprint ends prior to the antenna mounting area shown above.

Evaluation Kit

General Description

The GRBTM-EVA/GRBTM-EVNA evaluation boards provide a platform for evaluating the capabilities of the GRBTM-ANT-01 and GRBTM-NANT-01 modules for product applications. The board design includes three lateral 16-pin headers and one 12-pin header that provide easily accessible breakout connections to the module. The inner two headers maintain arduino compatibility for a simple start to any project. The evaluation boards support the following additional features:

- Bluetooth SMA Connector (GRBTMEV-NANT-01 variant only)
- Micro SD Card Interface
- USB 2.0 Micro B Communications Interface
- Power provided through USB, Battery Connection Header, or associated breakout pins
- USB-powered battery charger
- On-Board 1.8V and 3.3V Regulators
- Four general purpose LEDs
- One general purpose and One MCU RESET Push Button Switch
- 10-Pin SWD/MAXDAP Connection Header
- 1-Wire Secure Authenticator IC
- 1.8V I2C Accelerometer

GETTING STARTED

Procedure

Follow the steps below to verify board operation.

1. Carefully remove the evaluation board from its packaging while maintaining safe ESD practices.
2. Using the provided Micro USB B cable, power the device
3. Connect the Maxim MAX32625PICO# debugger to the eval board via the 10-pin ribbon cable.
4. Open eclipse or compatible IDE and program the board over the debugger with the MAX32666 BSP example projects.

Description of Hardware

Breakout Headers

JH3		JH4		JH5		JH6	
Pin	**Details**	**Pin**	**Details**	**Pin**	**Details**	**Pin**	**Details**
1	GND	1	VBATT	1	3.3V	1	P1.15
2	P0.9/UART TX	2	PWR ENABLE	2	VBATT	2	P1.14
3	P0.10/UART RX	3	VBUS	3	NC	3	P1.6
4	P0.26/MISO	4	P0.12/OWM	4	VBUS	4	P0.29
5	P0.25/MOSI	5	P0.3/SCK	5	P0.23	5	P0.30
6	P0.27/SCK	6	P0.5/SDIO3	6	P1.8	6	P0.31
7	P0.21/AIN5	7	P0.4/SDIO2	7	P1.9	7	P0.28
8	P0.20/AIN4	8	P0.2/SDIO1	8	P1.10	8	P1.13
9	P0.19/AIN3	9	P0.1/SDIO0	9	P0.22	9	P1.12
10	P0.18/AIN2	10	P0.0/SS0	10	P1.11	10	P1.4
11	P0.17/AIN1	11	PO.6/SCL	11	P0.13	11	P1.2
12	P0.16/AIN0	12	P0.7/SDA	12	P0.14	12	P1.3
13	GND	13	N/A	13	P0.24	13	P1.1
14	NC	14	N/A	14	P0.8	14	P1.0
15	3.3V	15	N/A	15	P0.15	15	P1.5
16	RSTN	16	N/A	16	P0.11	16	P1.7

Power Supply
The evaluation board is powered with +5VDC through the VBUS on the Micro-USB connector, pin 3 of the JH4 header, or through the Battery connector JH1. While charging a connected battery, a yellow LED (D3) will illuminate).

Current Monitoring
The evaluation board provides a 2-pin jumper header from 3.3V to the module for convenient current monitoring.

Universal Serial Bus
The provided USB connector allows the user to test various prototype USB slave applications.

UART Interfaces
The evaluation board does not provide any UART translation. The provided UART breakouts will require an external USB-to-UART bridge.

Bluetooth 5 Interface
The evaluation board with the module variant GRBTM-NANT-01 includes an SMA connector for access to the Bluetooth Tx-line.

For the variant GRBTM-ANT-01, the Bluetooth interfaces through the chip antenna embedded onto the module.

JTAG Serial Wire Debug (SWD) Support
SWD can be accessed through an ARM standard Cortex® 10-pin connector (JH2).

Pushbuttons
The pushbutton SW2 manually resets the MAX32666 MCU. Pushbutton SW1 is connected to the GPIO P1.10 of the module.

GPIO LEDs
The indicator lights are controlled by various pins as follows; P0.31 - D4 (Green), P0.30 - D4 (Blue), P0.29 - D4 (Red), P0.28 - D5 (White).

GPIOs
The provided GPIO breakouts function at 3.3V logic levels accessible through various pins on the lateral headers. For more details, refer to the MAX32666 User Guide.